MULTIMEDIA UNIVERSITY ™

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 1, **2017/2018**

EEE 3156 DIGITAL SYSTEMS

(EE Group)

25 OCTOBER 2017

2:30 PM – 4:30 PM
(2 Hours)

INSTRUCTION TO STUDENT

1. This Question paper consists of 4 pages including cover page with 4 Questions only.

2. Attempt **ALL FOUR** questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please print all your answers in the Answer Booklet provided.

Question 1:

(a) Analyze the circuit shown in Figure Q1 and compute the function, F.

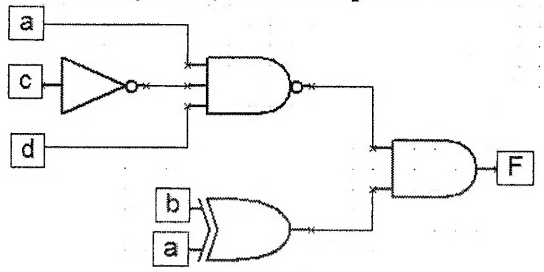

Figure Q1

[2 marks]

(b) Create the truth table of the function, F from part (a).

[8 marks]

(c) Compute the simplified sum of product and product of sum equations for function, F from part (b).

[8 marks]

(d) Design the simplified function, F from part (c) using:-

(i) Three-input look up tables only.

[3 marks]

(ii) Pure NAND gates only.

[4 marks]

Question 2:

Analyze the state diagram shown in Figure Q2 that consists of an input signal, w and an output signal, z.

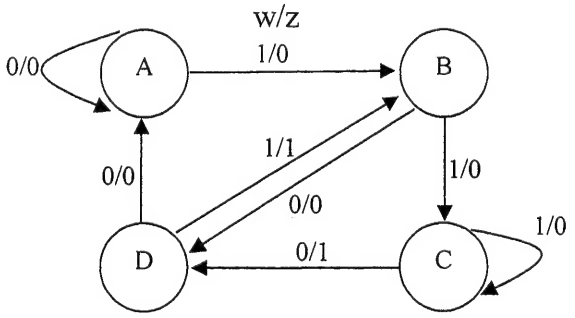

Figure Q2

(a) Create the state table of the system shown in Figure Q2.

[4 marks]

(b) Create the state assigned table of the system shown in Figure Q2.

[4 marks]

(c) Compute the simplified characteristic equations of the system shown in Figure Q2.

[11 marks]

(d) Based on the simplified equations computed in part (c), design the system shown in Figure Q2 using logic gates and D flip-flops.

[6 marks]

Continued ...

Question 3:

Refer to the circuit of an Arithmetic Logic Unit shown in Figure Q3.

(a) Create the truth table of the one stage of Logic Circuit. The logic operations of the one stage of Logic Circuit is shown in Table Q3.

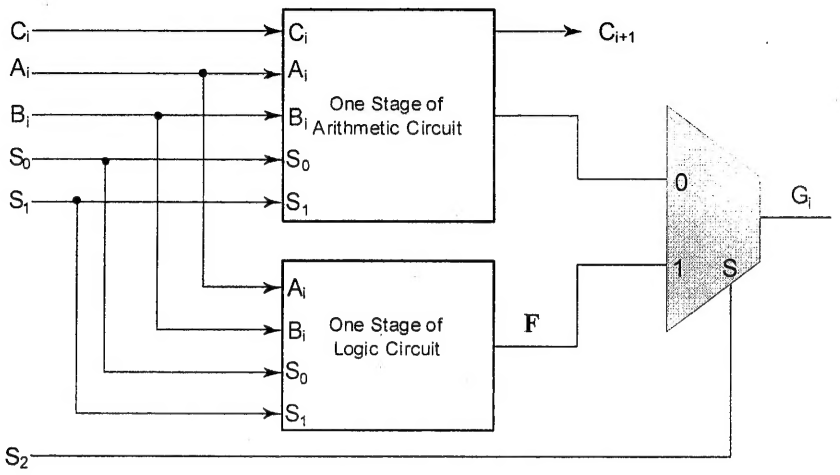

Figure Q3

Table Q3

S_1S_0	Logic operation, F
00	A and B
01	A or B
10	A xor B
11	not A

[4 marks]

(b) Compute the simplified characteristic equation of function F from part (a).

[8 marks]

(c) Design the one stage of Logic Circuit shown in Figure Q3 using Programmable Logic Arrays.

[8 marks]

(d) Design the one stage of Logic Circuit shown in Figure Q3 using logic gates and multiplexer.

[5 marks]

Continued ...

Question 4:

(a) Analyze the following instructions and state the type of data hazards (Read after Write, RAW, Write after Read, WAR, and Write after Write, WAW) that exist between the following instructions that executed in a 5-stages pipelined system.

i1: Add R1, R2, R3
i2: Add R4, R1, R4
i3: Add R3, R1, R2
i4: Add R1, R1, R4

[6 marks]

(b) Refer to the reservation table shown in Table Q4.

Table Q4

	t_0	t_1	t_2	t_3	t_4
Stage 1	X				X
Stage 2				X	
Stage 3		X	X		

(i) Compute the forbidden list.

[1 mark]

(ii) Compute the collision vector.

[1 mark]

(iii) Create the state diagram.

[6 marks]

(iv) Compute the minimum average latency.

[5 marks]

(c) Analyze the circuit shown in Figure Q4 and compute the mean time between failure of this circuit. Given that the clock frequency = 30 MHz, asynchronous transition rate = 2 MHz, setup time = propagation delay = 10 ns for all flip-flops. For 74ALS74, $\tau = 1$ ns, $\tau_0 = 8.7 \times 10^{-6}$ s and $t_r = 41.07$ ns.

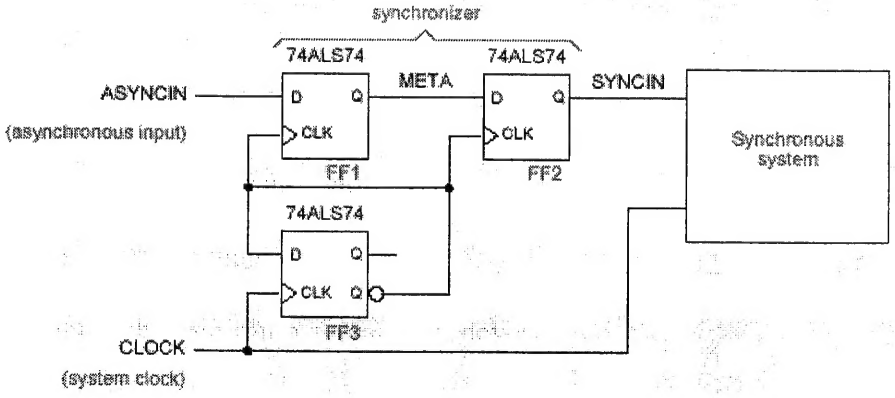

Figure Q4

[6 marks]

End of Paper